LOW POWER 256K MRAM DESIGN

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ABSTRACT

From the original Anisotropic Magneto-Resistance (AMR) readout design to the now popular Spin Dependent Tunneling (SDT) designs, Magnetoresistive Random Access Memory (MRAM) has evolved through a number of different materials and design concepts. Throughout this evolution, one common characteristic has been the use of 2D magnetic selection for writing the memory cell. In 2D magnetic selection, the combination of two orthogonal currents, each generating a magnetic field, is used to selectively write a single bit within an array of bits. 2D magnetic selection, due to the half-select condition that it places on the cells along a selected row and column, requires tight control over, or wide margins for, the magnetic switching characteristics of the cells. This requirement on the magnetic switching characteristics has led to yield problems in the design and manufacture of MRAM devices. In addition, MRAM designs that use 2D magnetic selection require high write currents because of the need for two separate write currents, the relatively low field generating efficiency of a write line that is separate from the storage element, and the magnetic switching process in the typical single magnetic storage film. A new SDT cell design incorporates a sandwich free layer and a write select transistor. For this cell, only a single write current, passing through the cell, is required for writing. Due to the magnetic switching characteristics of the antiferromagnetically coupled sandwich free layer, and the fact that only a single current is required, the write current requirement of this new cell is significantly lower that that of other MRAM designs. Also, the inclusion of a write select transistor in the cell eliminates the half-select disturb conditions that are found in other MRAM designs. Elimination of the half-select condition practically eliminates concerns with magnetic switching distributions and margins. Proof-of-concept sandwich-SDT devices exhibit write currents between 2 mA and 3 mA, in devices with a 2 μm minimum dimension. 0.6 μm devices are expected to switch at < 1 mA. This paper details the design and operation of the new sandwich-SDT MRAM cell, presents a differential memory architecture that uses this cell, and describes a byte wide, 256k memory design.